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Patentanmeldung Nr. Patent application No. Demande de brevet n°

03300216.3

Der Präsident des Europäischen Patentamts;
Im Auftrag

For the President of the European Patent Offic

Le Président de l'Office européen des brevets
p.o.

R C van Dijk

Anmeldung Nr:
Application no.: 03300216.3
Demande no:

Anmeldetag:
Date of filing: 14.11.03
Date de dépôt:

Anmelder/Applicant(s)/Demandeur(s):

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Bezeichnung der Erfindung/Title of the invention/Titre de l'invention:
(Falls die Bezeichnung der Erfindung nicht angegeben ist, siehe Beschreibung.
If no title is shown please refer to the description.
Si aucun titre n'est indiqué se referer à la description.)

Semiconductor device with a resonator

In Anspruch genommene Priorität(en) / Priority(ies) claimed /Priorité(s) revendiquée(s)
Staat/Tag/Aktenzeichen/State/Date/File no./Pays/Date/Numéro de dépôt:

Internationale Patentklassifikation/International Patent Classification/
Classification internationale des brevets:

H03H/

Am Anmeldetag benannte Vertragstaaten/Contracting states designated at date of filing/Etats contractants désignées lors du dépôt:

AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HU IE IT LU MC NL
PT RO SE SI SK TR LI

Semiconductor device with a resonator

FIELD OF THE INVENTION

The present invention relates to a method for fabricating a resonator within a semiconductor device, said semiconductor device comprising a substrate, and to an associated semiconductor.

Such a method may be integrated in, for example, a fabrication of a RF transceiver.

BACKGROUND OF THE INVENTION

A method for fabricating a resonator within a semiconductor device is described in the US patent application US 2002/0145489. Such a resonator provides an integrated oscillator with a very high Q factor that is needed to generate a stable frequency for the systems comprising a semiconductor device such as RF transceivers. Such a resonator is usually called Micro Electromechanical Device or MEM. Such a MEM is intended to replace discrete Quartz oscillators, which are costly devices and which can't be integrated within a semiconductor device. The semiconductor is based on an SOI (Silicon on Insulator) wafer comprising a substrate. An SOI wafer comprises an insulating layer generally made of oxide. The method for fabricating such a resonator comprises the steps of:

- defining a first layer born on the substrate,
- defining a second layer born on the substrate,
- etching the second layer to define an element capable of resonating in a vibrational mode, the element being approximated to a trench.

The oxide layer permits to stop the etching adequately and to avoid a coupling with the substrate, that is to say a leakage current. As shown in Fig. 33 of said prior art, the element is attached to the substrate at its bottom.

A first drawback of such a method is that it needs a specific complicated processing step after the realization of the resonator to make it hermetic. Indeed,

usually, at least one protective oxide layer and at least one metallized layer covers the whole substrate. In the prior art described, there is a need to define additional cap layers in order to prevent the element to be cast into the metallized and oxide layers.

A second drawback is that the etching can't be deep because it is stopped by the oxide insulating layer, such layer being not deeply integrated inside the substrate of the wafer, from 0.5 to 2 microns, which is a limitation in such SOI technology.

Finally, it is a costly solution because it uses SOI wafer, which are known to be more expensive than conventional semi-conductor wafers.

SUMMARY OF THE INVENTION

Accordingly, it is an object of the invention to provide a method for fabricating a resonator within a semiconductor device, said semiconductor device comprising a substrate, and a semiconductor device, which allow to perform the fabrication of a resonator and the hermeticity of the semiconductor device in the same time and in a simple way without using an SOI wafer.

To this end, there is provided a method for fabricating a resonator within a semiconductor device, said semiconductor device comprising a substrate with a first and a second axes which are perpendicular, wherein said method comprises the steps of:

- Etching a hole in the substrate,
- Creating a first doping zone for defining a first electrode,
- Partitioning said first electrode into two electrodes,
- Applying a delimited oxide deposit inside and around the hole according to a specific deposit pattern,
- Defining a second doping zone covering totally the hole,
- Removing the oxide deposit in order to define an element forming the resonator able to vibrate between the two electrodes.

In addition, there is provided a semiconductor device comprising a substrate with a first doping zone, two perpendicular axes, a second doping zone in contact with the first doping zone and a resonator, said resonator being represented by an

element with two parts able to vibrate between two electrodes made of the first doping zone, the first part of said element being held substantially planar to the substrate's surface by means of the second doping zone and the second part of said element being substantially perpendicular to the substrate's surface and free of movements.

As we will see in detail further on, the oxide zone used in the method permits to obtain an element able to vibrate between two electrodes, said element being in a hole, whereas the second doping layer covers the hole so as to make the hermeticity of the resonator, and at the same time to maintain one part of the element attached to the surface of the substrate.

Preferably, in a non-limited embodiment, said hole is a trench or a pore, which is substantially perpendicular to the surface of the substrate.

Advantageously, the substrate is a high ohmic type and the first doping zone is a low ohmic type.

Preferably, in a non-limited embodiment, the partitioning of the two electrodes is obtained by means of a partitioning pattern enabling argon or bore or ion implant.

Advantageously, the implant covers partially the hole at its bottom and sides and the substrate's surface neighboring said hole.

Advantageously, the specific deposit pattern extends along the second axe, the inside of said deposit pattern allowing the oxide to be settled inside the whole hole and at the substrate's surface neighboring said hole and beyond.

Advantageously, the second doping zone is obtained by means of a second doping pattern extending along the first axe of the semiconductor, the inside of said pattern allowing a second dopant to be settled totally inside the hole.

Advantageously, the inside of the second doping pattern permits a second dopant to cover totally the oxide deposit neighboring the hole and beyond.

Preferably, in a non-limited embodiment, said method comprises a further step of adding first pads along the second axe on both sides of the hole, said pads being in contact with the first doping zone.

Preferably, in a non-limited embodiment, said method comprises a further step of adding second pads along the first axe on both sides of the hole, said pads being in contact with the second doping zone.

BRIEF DESCRIPTION OF THE DRAWINGS

Additional objects, features and advantages of the invention will become apparent upon reading the following detailed description and upon reference to the accompanying drawings in which:

- Fig.1 is a flow chart of the method for fabricating a resonator within a semiconductor according to the invention,
- Fig.2 depicts a semiconductor used for making a resonator according to the method of Fig.1,
- Fig.3 illustrates a definition pattern applied on the semiconductor device of Fig.2,
- Fig.4 depicts two sectional views of the semiconductor device of Fig.2 after a pattern definition step,
- Fig.5 illustrates an etching pattern applied on the semiconductor device of Fig.3,
- Fig.6 depicts a sectional view of the semiconductor of Fig. 4 after an etching step and a first doping step,
- Fig.7 illustrates a partitioning pattern applied on the semiconductor device of Fig.5,
- Fig.8 depicts two sectional views of the semiconductor of Fig. 6 after a partitioning step,
- Fig.9 illustrates a delimited oxide deposit pattern applied on the semiconductor device of Fig.7,

- Fig.10 depicts two sectional views of the semiconductor device of Fig. 8 after an oxide deposit step,
- Fig.11 illustrates a doping pattern applied on the semiconductor device of Fig.9,
- Fig.12 depicts two sectional views of the semiconductor device of Fig. 10 after a second doping step,
- Fig.13 depicts two sectional views of the semiconductor device of Fig.12 after a cleaning step,
- Fig.14 is a plan view of the semiconductor device of Fig.11 with some added contacts, and
- Fig.15 depicts two sectional views of the semiconductor device of Fig.13 with some added contacts.

DETAILED DESCRIPTION OF THE INVENTION

In the following description, well-known functions or constructions by the person skilled in the art are not described in detail since they would obscure the invention in unnecessary detail.

The present invention relates to method for fabricating a resonator within a semiconductor device SI. Said semiconductor device SI comprises a substrate Z_HO. Said substrate is made of silicon. A flow chart of said method is described in the Fig.1 and the semiconductor device SI is illustrated in Fig.2.

The substrate Z_HO is a high ohmic substrate, its resistivity being preferably greater than 10 Ohm.cm, so that it presents a high resistivity. The semiconductor device SI comprises two axes XX' and YY' that are perpendicular one to each other and that are planar to the surface of said semiconductor device SI.

For the following description two sectional views, represented on Fig.4, will be used, a first one AA' along the first axe XX' and a second one BB' along the axe YY' as shown in Fig.2.

In order to fabricate a resonator within said semiconductor device SI, the following steps are performed.

In a first step DEFINITION), a first definition zone Z_HL is defined onto the semiconductor device SI by means of a first pattern M_HL called definition pattern. The resonator will be built in this definition zone Z_HL. The definition

pattern M_HL serves as an isolation layer to protect the area outside the resonator device during the next process step.

To this end, the first pattern M_HL is applied onto the substrate of the semiconductor device SI, the inside of the pattern being open and being the definition zone Z_HL and the outside being a plain mask, said first pattern covering partially the substrate of the semiconductor device SI. This first pattern M_HL extends along the second axe BB' as shown in Fig.3.

As usually known, a physical mask that represents a specific pattern is made of borosilicate. Two different methods are used whether a resin or an oxide is to be settled on the substrate.

If a resin is applied on the substrate, the following method is used.

- The resin is applied on the substrate,
- The mask is applied,
- The whole substrate is exposed to the UV,
- The resin layer, which is a photo-resist that is suited to UV or X-ray exposure, polymerized under said exposure where it is not masked,
- The resin is developed,
- Some metallized layers, etching etc, ... are performed on the substrate, and
- The resin is removed with a solvent.

It is to be noted that when a resin is developed, the whole substrate is dived into a develop product known to those skilled in the art. Said product dissolves the zones where the resin has polymerized. Thus, the substrate comprising two kind of zones: some stripped zones and some protected zones.

If an oxide is applied, the following method is used.

- The oxide is applied on the whole surface of the substrate,
- A resin is applied on the oxide and the mask is applied,
- The whole substrate is exposed to the UV,
- The resin layer is developed after polymerization, thus some oxide zones are stripped,
- The stripped oxide zones are etched (ionic etching) so that the oxide in these zones is removed, and

- The resin is removed with a solvent; the substrate has therefore some zones covered with oxide representing a pattern identical to the mask applied.
- Finally, some doping or etching can be performed for example, and then the remaining oxide can be removed by etching.

It is to be noted that this second method also called hard mask is used whenever a resin is not enough firm to bear a step of deep etching for example.

In a second step ETCHTING), a hole TR is performed inside the substrate of the semiconductor device SI by means of a second pattern M_TR. As illustrated in Fig.5, the second pattern M_TR (a rectangle in a continuous line) is smaller than the first pattern M_HL and is applied inside the outlines of the first pattern M_HL so that the hole TR is performed inside the definition zone Z_HL.

The hole is a trench of a pore. The hole is substantially perpendicular to the surface of the substrate, as shown in Fig.6 on the sectional view BB'.

In a third step FIRST DOPING), a first doping is performed onto the substrate inside the definition zone Z_HL to have a low access resistance so that a conductive area or first doping zone Z_DIFF1 that forms an electrode is defined. This first doping zone Z_DIFF1 is low ohmic with a resistivity being preferably smaller than 0.5 Ohm.cm. Thus, a part of the definition zone becomes a low ohmic zone after this first doping step.

The first doping zone Z_DIFF1 is represented by the areas filled with points as shown in the sectional view BB' of Fig.6.

The doping is performed with a dopant of ions N+ for example. Thus, the first doping zone Z_DIFF1 forms a crystalline network made of ions N+.

The definition pattern M_HL, which is a hard mask, is then removed.

In a fourth step PARTITION), a partitioning of the conductive area Z_DIFF1 is performed in order to have two distinct conductive areas. To this end, a third pattern M_ARBOR is used in order to apply a dopant that is highly resistive inside the hole TR. The dopant is preferably made of Boron or Argon AR or ion. As shown in the planar view of Fig.7, the third pattern M_ARBOR is represented by two

squares in continuous lines, the inside of the squares being plain. This pattern M_ARBOR extends along the second axe YY'.

The arrows in the sectional views AA' or BB' of Fig.8 show the areas where a deposit of Boron or Argon is to be performed. The grey areas show where there is effectively a deposit of Boron or Argon. The deposit is performed on the whole surface of the semiconductor device SI except the surface hidden by the third pattern M_ARBOR. It covers partially the outlines and the bottom of the hole. The pattern M_ARBOR is such that it lets the Argon settled partially inside the bottom and on the sides of the hole TR and partially at the surface of the substrate in the neighborhood of said hole TR.

In more details, in the first sectional view AA', outside the hole TR at the surface of the substrate, one can see that the Argon settled at the surface of the substrate and covers totally the substrate neighboring the hole TR, whereas in the second sectional view BB', outside the hole TR at the surface of the substrate, the dopant AR doesn't settled on the first doping zone Z_DIFF1 but next to this zone, directly on the substrate Z_HO.

Thus, the deposit of the highly resistive dopant defined two distinct conductive areas inside the hole made of the first dopant Z_DIFF1, which form two electrodes ELECT1, and ELECT2 as illustrated in Fig.8. Indeed, the Argon or Boron implant in the bottom of the hole TR permits to break the atomic links of the crystalline network. Thus, the conductivity of the silicon that was doped with some ions N+ is annihilated at this location.

After the Argon deposit, the third pattern M_ARBOR is removed from the substrate by etching as described before in the mask description.

In a fifth step OXIDE DEPOSIT), a delimited oxide deposit Z_OXI is performed onto the substrate of the semiconductor device SI, said oxide deposit being used to later define an element that represents the resonator as will be described below.

To this end, a fourth specific delimited pattern M_ONO is applied on the substrate of the semiconductor device SI. This fourth pattern is shown in Fig.9 in small points and lines and extends along the second axe YY'. It covers totally the

former locations of the first M_HL, second M_TR and third patterns M_ARBOR. The inside of said oxide deposit pattern M_ONO represents the openings that allow the oxide to be settled, the outside being the plain mask.

The pattern is such that it lets the oxide settled inside the whole hole TR and at the surface of the substrate neighboring the hole TR and beyond, so that it covers totally the low ohmic zone Z_HL.

The oxide deposit Z_OXI is illustrated in details in the sectional views AA' and BB' of Fig.10 and is represented by the squared areas. As can be seen, inside the hole TR, the oxide Z_OXI is settled at its bottom and on its sides.

Moreover, as can be seen in the first sectional view AA', outside the hole TR at the surface of the substrate, the oxide is settled on the argon implant in the neighborhood of the hole TR. In the second sectional view BB', outside the hole TR at the surface of the substrate, the oxide Z_OXI covers totally the first doping zone Z_DIFF1 neighboring the hole TR and covers the Argon implant neighboring this part of the first doping zone Z_DIFF1.

In a sixth step SECOND DOPING), a second doping with a second dopant is performed.

To this end, a fifth pattern M_PS is applied on the substrate of the semiconductor device SI. This fifth pattern M_PS is illustrated in Fig.11 in small points. It extends along the first axe XX' of the semiconductor device SI so that it covers totally the former location of the second pattern M_TR, and partially the other former locations of the first M_HL, third M_ARBOR and fourth patterns M_ONO. The outside of the pattern M_PS represents the plain mask and the inside represents the openings that permit the second dopant, for example some ions P+, to be settled.

As can be seen in Fig.14, this second doping pattern M_PS permits to have two openings PS1 and PS2 that don't cover the former locations of the other patterns so that some pads can be added later on at the location of these two openings PS1 and PS2.

The dopant deposit Z_DIFF2 is illustrated in details in the sectional views AA' and BB' of Fig.12 and is represented by the hatched areas. As can be seen,

inside the hole TR, this second dopant Z_DIFF2 is settled at its bottom and on its sides.

Moreover, as can be seen in the first sectional view AA', outside the hole TR at the surface of the substrate, the second dopant Z_DIFF2 covers totally the oxide deposit Z_OXI neighboring the hole TR and covers the Argon implant next to this oxide deposit part. In the second sectional view BB', outside the hole TR at the surface of the substrate, the dopant Z_DIFF2 covers partially the oxide zone Z_OXI neighboring the hole TR.

Of course, the second dopant for the second doping zone Z_DIFF2 can also be made of some ions N+. In this case, the first dopant for the first doping zone Z_DIFF1 is made of some ions P+.

In a seventh step CLEANING), the oxide deposit is removed in order to define the element, said element being able to vibrate between the two electrodes defined in the fourth step, and thus representing the resonator. The cleaning is performed with a solvent of fluoridric acid, for example. Thus, at the location of the oxide, there is now some air AIR as shown on the Fig.13.

As shown on the sectional views AA' and BB' of the semiconductor device SI, said element comprised two parts, the first part M1 of said element being held substantially planar to the surface of the substrate and the second part M2 of said element being substantially perpendicular to the surface of the substrate and free of movements. The first part M1 is attached to the surface by means of the second doping zone Z_DIFF2 as can be seen on the first sectional view AA'. As can be also observed in the second sectional view BB', the second part M2 that is vertical is free of movements, so that the element is easily able to vibrate between the two electrodes ELEC1 and ELEC2 when these electrodes are excited by a current, the element being made of the second doping zone Z_DIFF2.

Thus, it is to be noted that this second doping zone Z_DIFF2 permits to make the resonator hermetic and therefore the substrate of the semiconductor device SI, as it extends beyond the hole TR where the element is located as described before, and

beyond the oxide deposit neighboring the hole TR as shown in the first sectional view AA'.

In an additional step ADD PADS), first pads CTA are added in order to be able to apply a current for making the element vibrates as shown in Fig.14. Hence, electrical access is provided to the resonator. Two first pads CTA are added along the second axe YY', which are in contact with the first doping zone Z_DIFF1 as shown in the second sectional view BB', represented on Fig.15. The two contacts are on both sides of the hole TR.

Thus, in order to start a vibration phenomenon, AC and DC voltages are applied onto these two pads CTA. A capacitive coupling is performed as the two electrodes ELEC1 and ELEC2 are excited by the voltages furnished, current can easily circulate going through the low resistive electrodes (that are made of the first doping zone Z_DIFF1).

In response, the element inside the hole TR will mechanically vibrate as it is made of a second dopant Z_DIFF2, which is opposite to the one Z_DIFF1 of which are made the two electrodes. When the signal frequency of the AC voltage matches the vibration, the resonator resonates.

Finally, in order to recover the vibration of the element, two other pads CTB are added along the first axe XX', which are in contact with the second doping zone Z_DIFF2 that neighbored the first part M1 of the element as illustrated in the first sectional view AA'. The two contacts CTB are on both sides of the hole TR.

More specifically these pads CTB are connected at the location of the two openings PS1 and PS2 of the fourth pattern M_PS used as illustrated in Fig.14. An AC signal can be detected at these second two pads CTB via an amplifier (not represented) connected to these second two pads CTB.

In an additional step), an oxide layer Z_RES is added onto the second doping zone Z_DIFF2 and onto the whole substrate in order to protect the substrate of the semiconductor device SI. Thus, the hole TR is completely filled in and the second vertical part M2 of the element includes also a part of the oxide layer Z_RES added as shown in Fig.15. Of course, the first CTA and second CTB pads are defined in this layer Z_RES such that said layer lets these contacts free to be connected.

Finally, as usually known, many metallized layers and oxide layers are added onto the substrate of the semiconductor device SI, the last oxide layer being a protection layer, and metal pins are connected in order to connect the semiconductor to an electric housing. It is to be noted that the metallized layers are used to connect some pads to have access to some components of said semiconductor such as resistances, inductances and capacitances, and that the oxide layers are used as insulating layers between the metallized layers.

It is to be noted that thanks to the second doping zone Z_DIFF2 that makes the element of the resonator hermetic, said element is still free of movements although there are some other layers added on the substrate.

It is to be noted that this method for fabricating a resonator within a semiconductor device can be integrated in a method for fabricating an integrated circuit that comprises other functionalities than the resonator.

Thus, a resonator with good Q factor is fabricated in a simple way. Indeed, the distance between the two electrodes and the element of the resonator is very small, from 0.1 to 1μm (that is the thickness of the oxide deposit M_OXI), which permits to have an efficient coupling with no energy loss. The element mechanically vibrates at a precise frequency. Thus, the slight resistive loss associated to a pure vibration permits to have a good resonance frequency. It is known that the Q factor is inversely proportional to the resistances.

Another advantage is that in the same time the resonator is fabricated, the hermeticity of the resonator and thus of the substrate is performed with no added processing step contrary to the prior art, where another complex processing step is needed to perform the hermeticity of the substrate. Indeed, it is the second doping zone Z_DIFF2 that permits to protect the element of the resonator from the other layers by as it extends beyond the hole TR.

Moreover, no costly semiconductor is used as no SOI technology is needed in the invention. Thus, a deep hole can be dig up into the substrate, contrary to the prior art where the oxide insulating layer of the SOI technology prevents this.

A fourth advantage is that the two electrodes built are electrically protected against the substrate of the semiconductor device. Indeed, there is no leakage current

as the electrodes are low resistive compared to the substrate that is highly resistive. The current goes through the less resistive path which is represented by the electrodes.

A fifth advantage is that the resonator is integrated in the semiconductor itself, which is better than having an external discrete resonator, as it allows drastically size and cost reductions.

A sixth advantage is that this resonator takes lower space in the semiconductor than those which are based on a planar technology such as bulk acoustic silicon resonator where the resonator is put horizontally to the surface of the semiconductor and vibrates according to a flexural mode.

Finally, another advantage is that the fabrication of the resonator takes place during an integration silicon process, that is to say at the same time a semiconductor is fabricated. Indeed, a semiconductor device provides some capacitances, resistances and inductances. The capacitances are obtained with the trench TR and the first doping zone Z_DIFF1 as described before, the resistances are obtained with the second doping zone Z_DIFF2, and the inductances are obtained with the metallized layers. Additional diffusion layers can be added to fabricate active devices such as transistors.

Of course, the fabrication of the resonator can be included also in a silicon process used for an active semiconductor with transistors.

It is to be understood that the present invention is not limited to the aforementioned embodiments and variations and modifications may be made without departing from the spirit and scope of the invention as defined in the appended claims. In the respect, the following closing remarks are made.

It is to be understood that the present invention is not limited to the aforementioned mobile phone application. It can be used within any application using a system with a voltage control oscillator where a drift frequency occurs, in automobile application for example.

It is to be understood that the method according to the present invention is not limited to the aforementioned implementation.

Any reference sign in the following claims should not be construed as limiting the claim. It will be obvious that the use of the verb "to comprise" and its conjugations do not exclude the presence of any other steps or elements besides those defined in any claim. The article "a" or "an" preceding an element or step does not exclude the presence of a plurality of such elements or steps.

CLAIMS

1. Method for fabricating a resonator within a semiconductor device, said semiconductor device comprising a substrate (Z_HO) with a first (XX') and a second (YY') axes which are perpendicular, wherein said method comprises the steps of :
   - Etching a hole (TR) in the substrate (Z_HO)
   - Creating a first doping zone (Z_DIFF1) inside and around the hole (TR) for defining a first electrode,
   - Partitioning said first electrode into two electrodes (ELEC1, ELEC2),
   - Applying a delimited oxide deposit (Z_OXI) inside and around the hole (TR) according to a specific deposit pattern (M_ONO),
   - Defining a second doping zone (Z_DIFF2) covering totally the hole (TR),
   - Removing the oxide deposit (Z_OXI) in order to define an element forming the resonator able to vibrate between the two electrodes (ELEC1, ELEC2).

2. Method for fabricating a resonator within a semiconductor device as claimed in claim 1, wherein said hole (TR) is a trench or a pore, which is substantially perpendicular to the substrate's surface (Z_HO).

3. Method for fabricating a resonator within a semiconductor device as claimed in claim 1, wherein the substrate (Z_HO) is a high ohmic type and the first doping zone (Z_DIFF1) is a low ohmic type.

4. Method for fabricating a resonator within a semiconductor device as claimed in claim 1, wherein the partition of the two electrodes (ELEC1, ELEC2) is obtained by means of a partitioning pattern (M_ARBOR) enabling argon or boron or ion implant.

5. Method for fabricating a resonator within a semiconductor device as claimed in claim 4, wherein the implant (AR) covers partially the hole (TR) at its bottom and sides and the substrate's surface neighboring said hole (TR).

6. Method for fabricating a resonator within a semiconductor device as claimed in claim 1, wherein the specific deposit pattern (M_ONO) extends along the second axe (YY'), the inside of said deposit pattern (M_ONO) allowing the oxide to be settled inside the whole hole (TR) and at the substrate's surface neighboring said hole (TR) and beyond.

7. Method for fabricating a resonator within a semiconductor device as claimed in claim 1, wherein the second doping zone (Z_DIFF2) is obtained by means of a second doping pattern (M_PS) extending along the first axe (XX') of the semiconductor (SI), the inside of said pattern (M_PS) allowing a second dopant to be settled totally inside the hole (TR).

8. Method for fabricating a resonator within a semiconductor device as claimed in claim 7, wherein the inside of said pattern (M_PS) permits a second dopant to cover totally the oxide deposit neighboring the hole (TR) and beyond.

9. Method for fabricating a resonator within a semiconductor device as claimed in claim 1, wherein said method comprises a further step of adding first pads (CTA) along the second axe (YY') on both sides of the hole (TR), said pads being in contact with the first doping zone (Z_DIFF1).

10. Method for fabricating a resonator within a semiconductor device as claimed in claim 1, wherein said method comprises a further step of adding second pads (CTA) along the first axe (XX') on both sides of the hole (TR), said pads being in contact with the second doping zone (Z_DIFF2).

11. Method for fabricating a resonator within a semiconductor device as claimed in claim 1, wherein said semiconductor device comprises a substrate (Z_HO) with a first definition zone (Z_HL) where the resonator is built.

12. Method for fabricating a resonator within a semiconductor device as claimed in claim 11, wherein said method is integrated in a method for fabricating an integrated circuit.

13. Semiconductor device comprising a substrate (Z_HO) and a first doping zone (Z_DIFF1), and two perpendicular axes (XX', YY') and a second doping zone (Z_DIFF2) in contact with the first doping zone (Z_DIFF1) and a resonator, said resonator being represented by an element with two parts able to vibrate between two electrodes (ELEC1, ELEC2) made of the first doping zone (Z_DIFF1), the first part (M1) of said element being held substantially planar to the substrate's surface by means of the second doping zone (Z_DIFF2) and the second part (M2) of said element being substantially perpendicular to the substrate's surface and free of movements.

Semiconductor device with a resonator

ABSTRACT

The present invention relates to a method for fabricating a resonator within a semiconductor device, said semiconductor device comprising a substrate, wherein said method comprises the steps of:

- Etching a hole in the substrate,
- Creating a first doping zone for defining a first electrode,
- Partitioning said first electrode into two electrodes,
- Applying a delimited oxide deposit inside and around the hole,
- Defining a second doping zone covering totally the hole,
- Removing the oxide deposit in order to define an element forming the resonator able to vibrate between the two electrodes.

Use: Semiconductor in RF Transceiver

Reference: Fig. 1

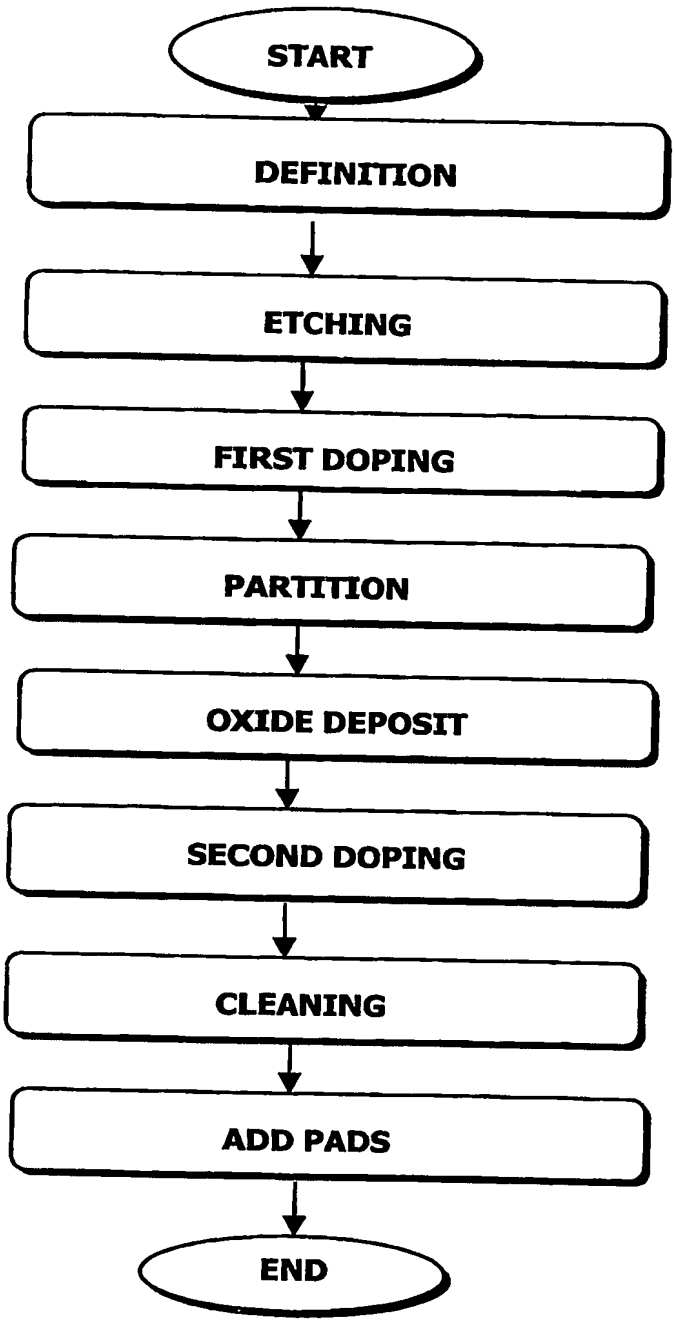
START
DEFINITION
ETCHING
FIRST DOPING
PARTITION
OXIDE DEPOSIT
SECOND DOPING
CLEANING
ADD PADS
END

FIG. 1

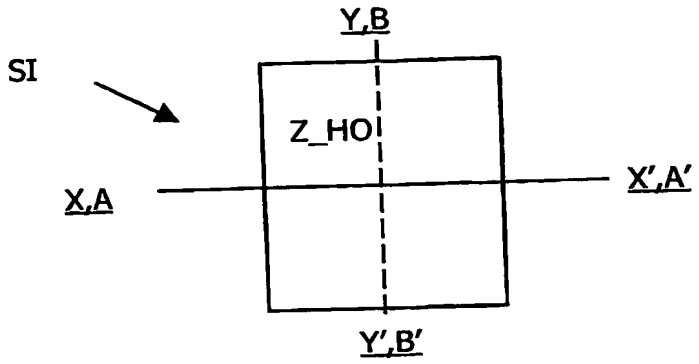

FIG. 2

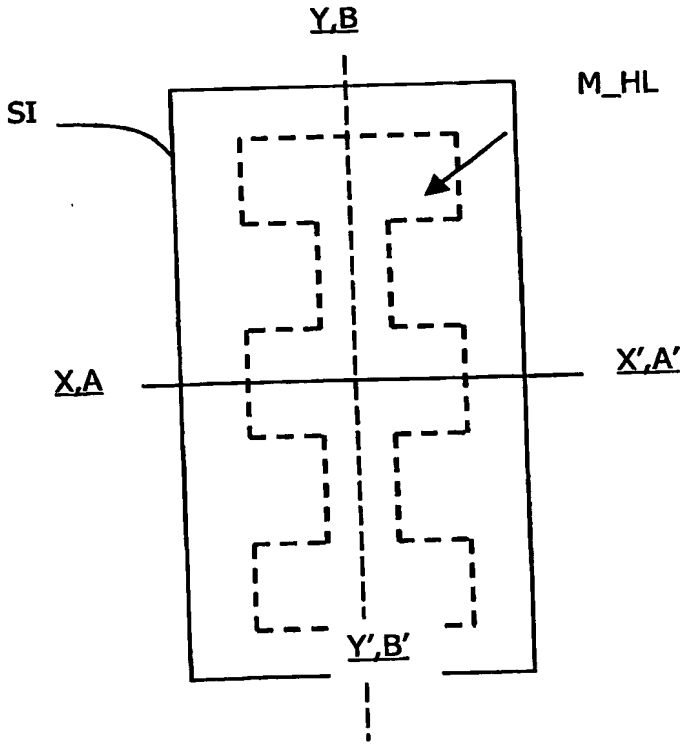

FIG. 3

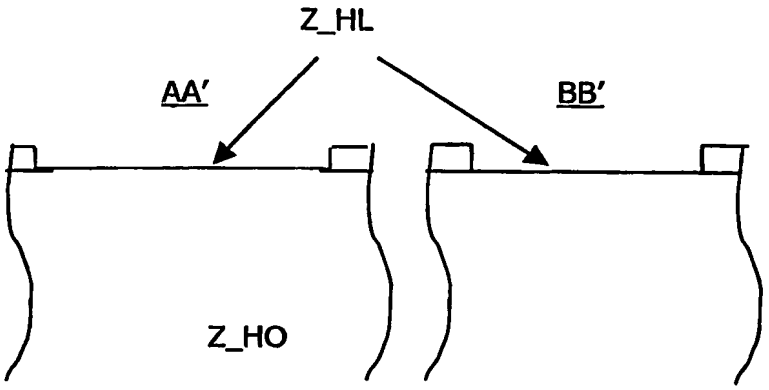

FIG. 4

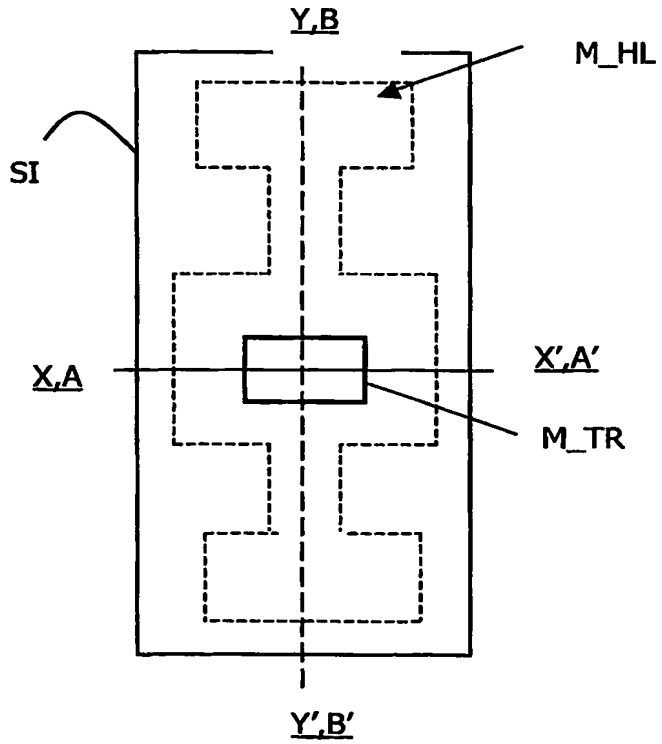

FIG. 5

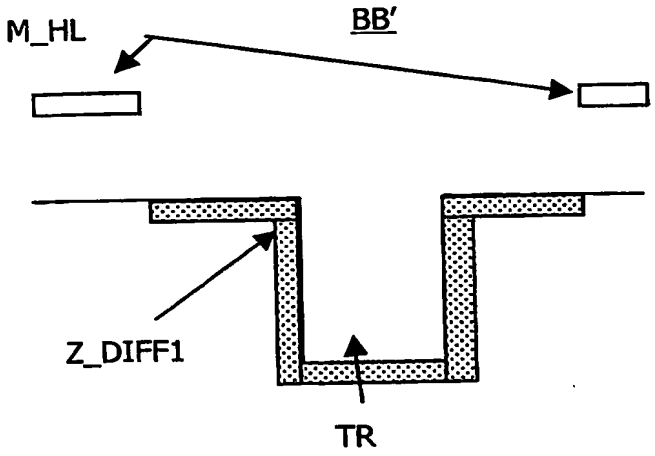

FIG. 6

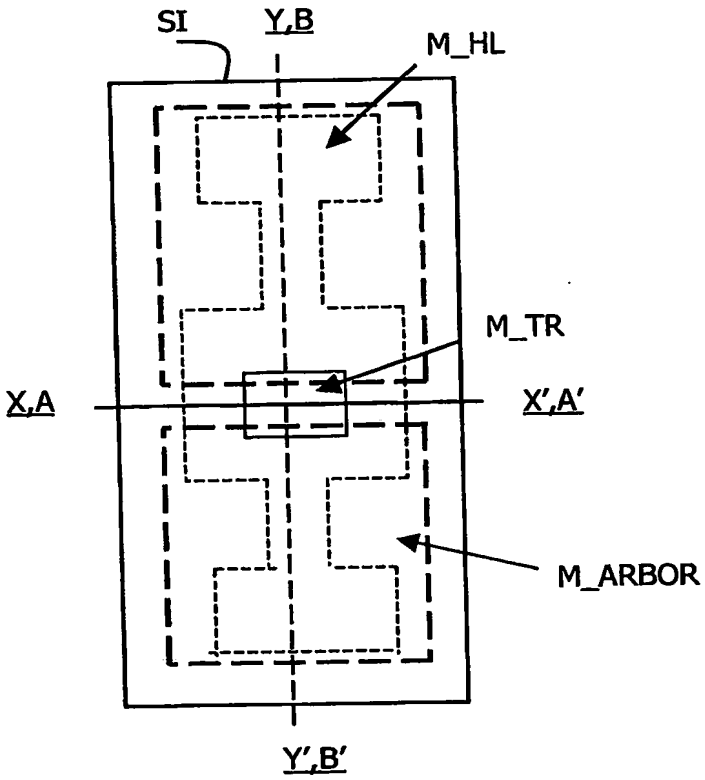

FIG. 7

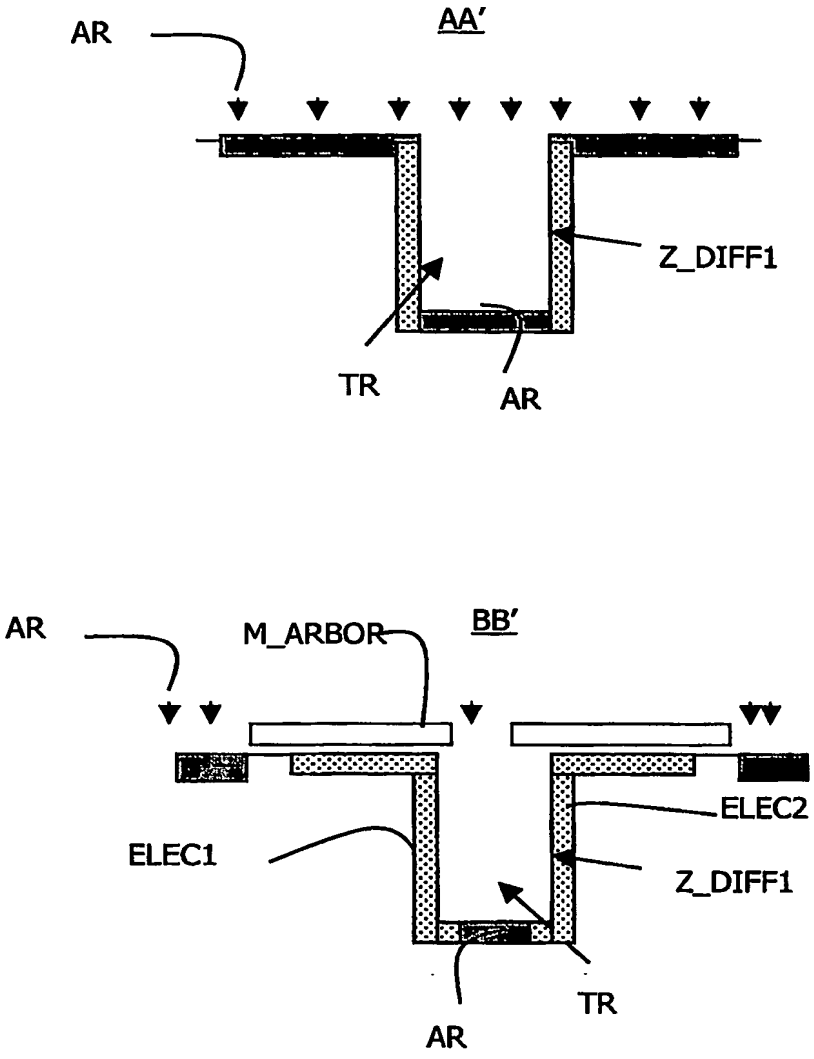

FIG. 8

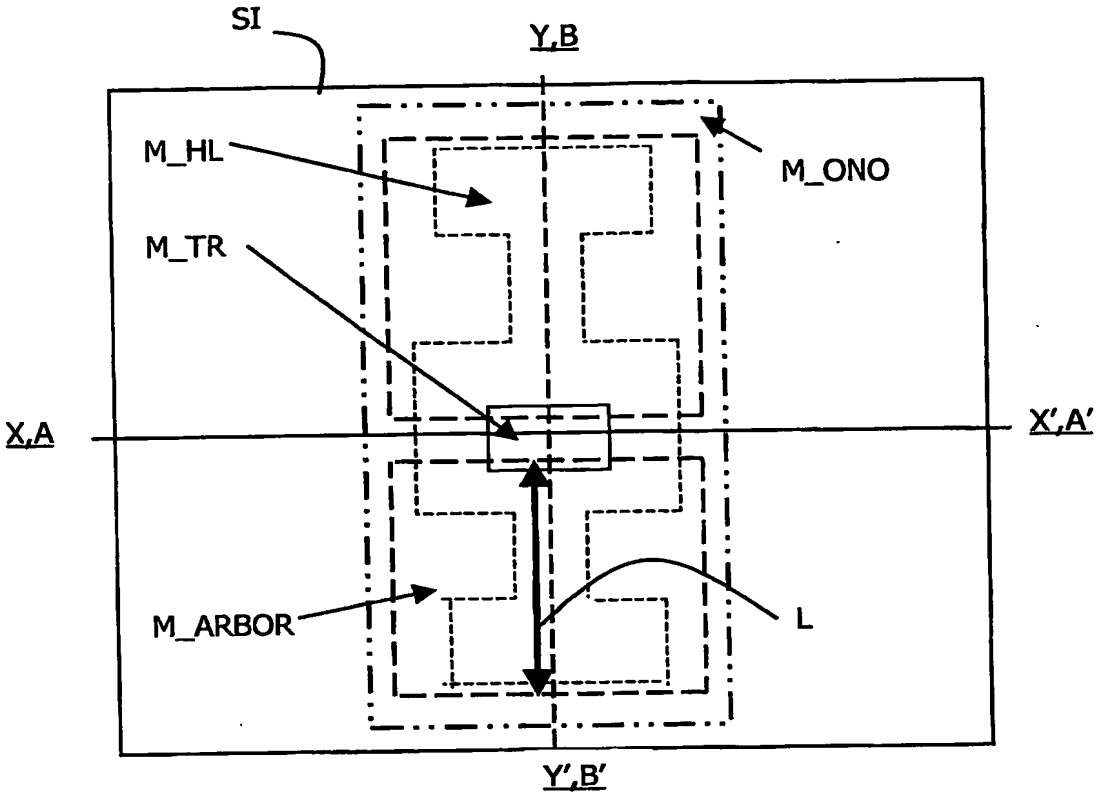
SI
Y,B
M_HL
M_ONO
M_TR
X,A
X',A'
M_ARBOR
L
Y',B'

FIG. 9

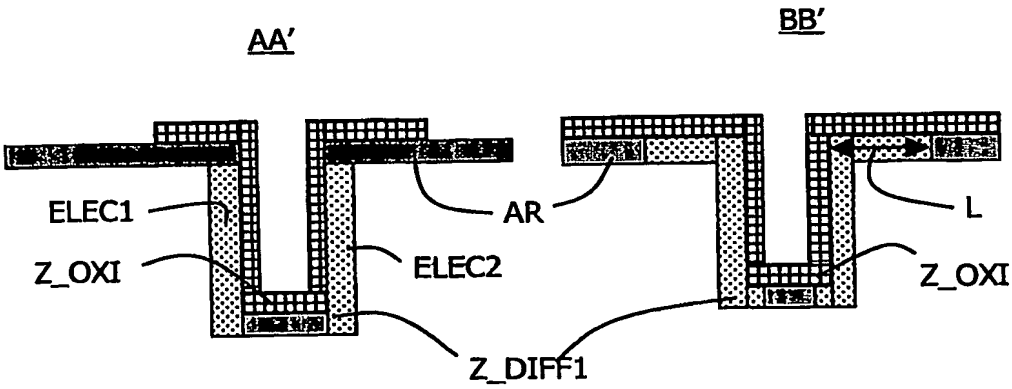
AA'
BB'
ELEC1
AR
L
Z_OXI
ELEC2
Z_OXI
Z_DIFF1

FIG. 10

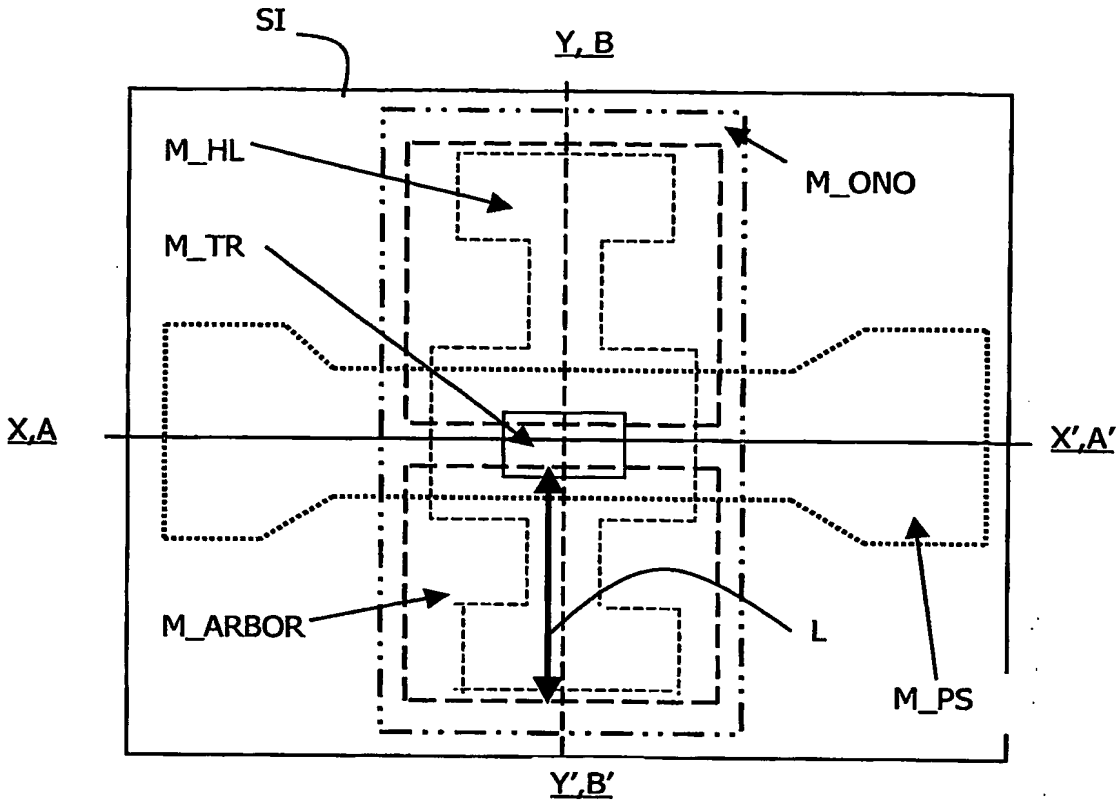
SI
Y, B
M_HL
M_ONO
M_TR
X,A
X',A'
M_ARBOR
L
M_PS
Y',B'

FIG. 11

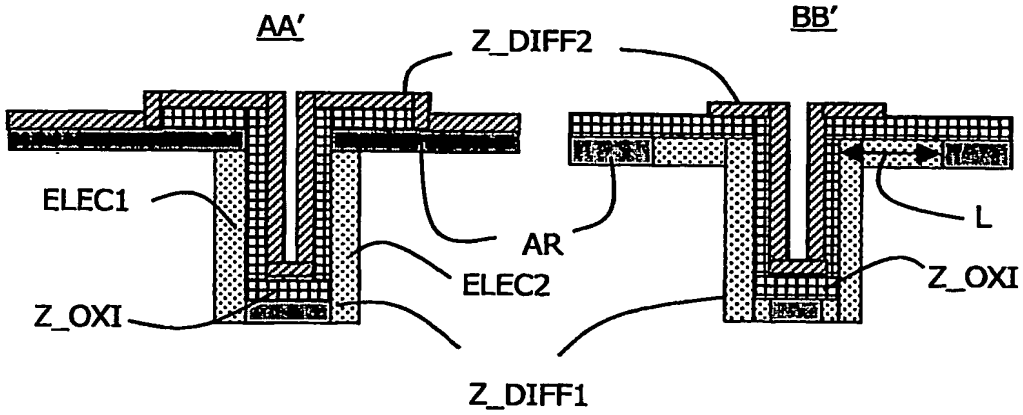
AA'
BB'
Z_DIFF2
ELEC1
AR
L
ELEC2
Z_OXI
Z_OXI
Z_DIFF1

FIG. 12

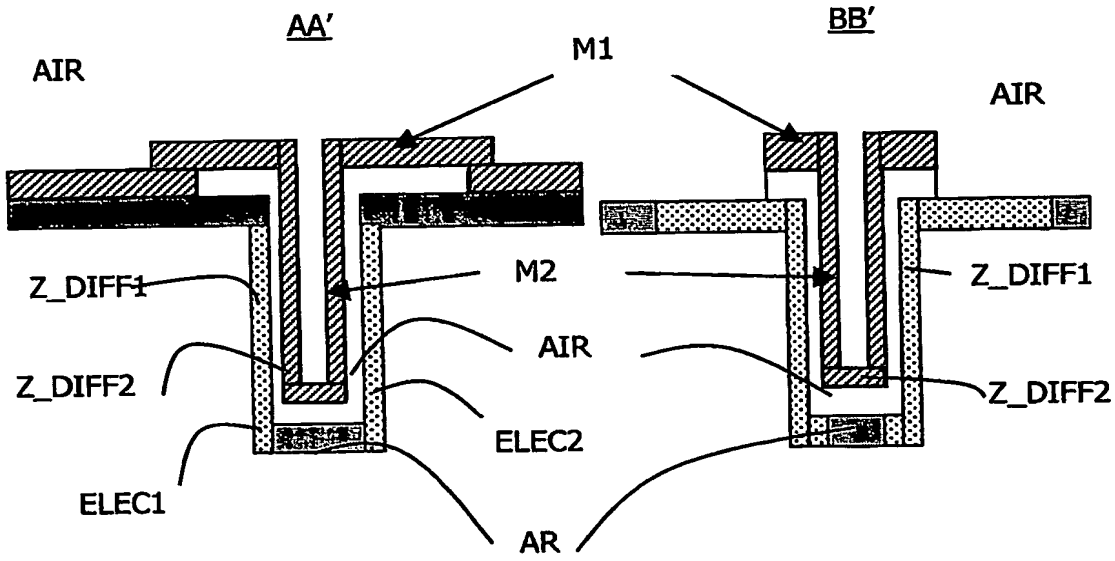
AA'
BB'
AIR
M1
AIR
Z_DIFF1
M2
Z_DIFF1
AIR
Z_DIFF2
Z_DIFF2
ELEC2
ELEC1
AR

FIG. 13

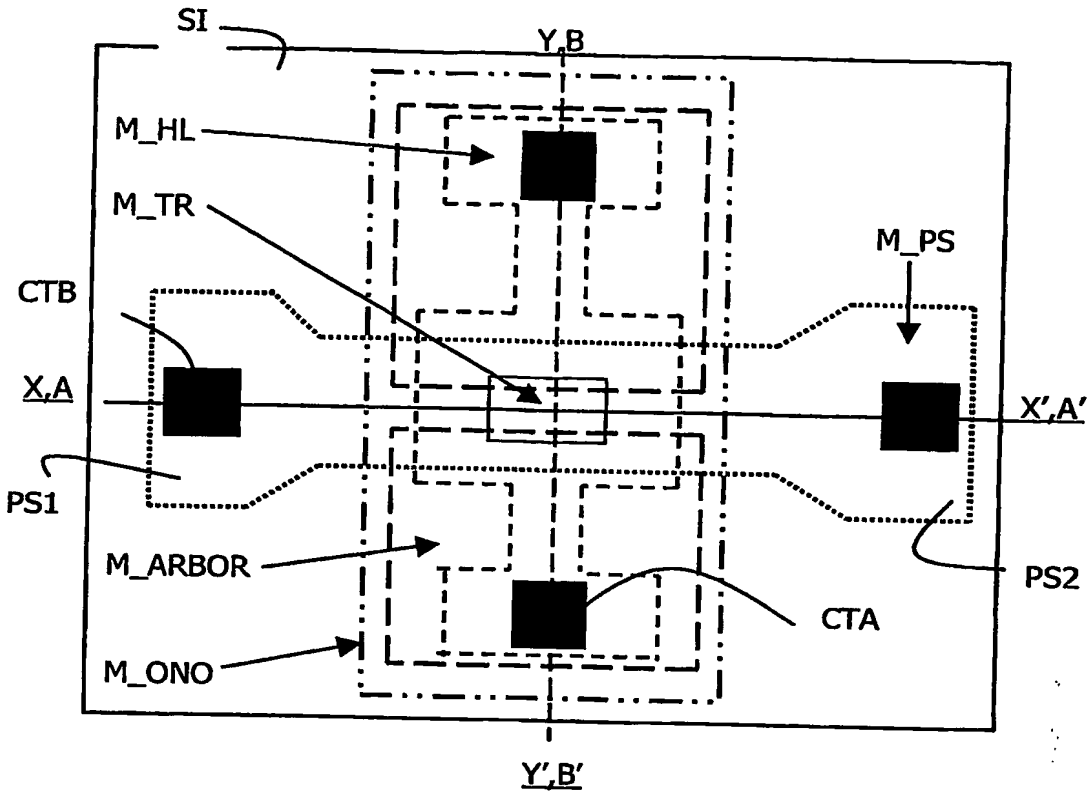
SI
Y,B
M_HL
M_TR
M_PS
CTB
X,A
X',A'
PS1
M_ARBOR
PS2
CTA
M_ONO
Y',B'

FIG. 14

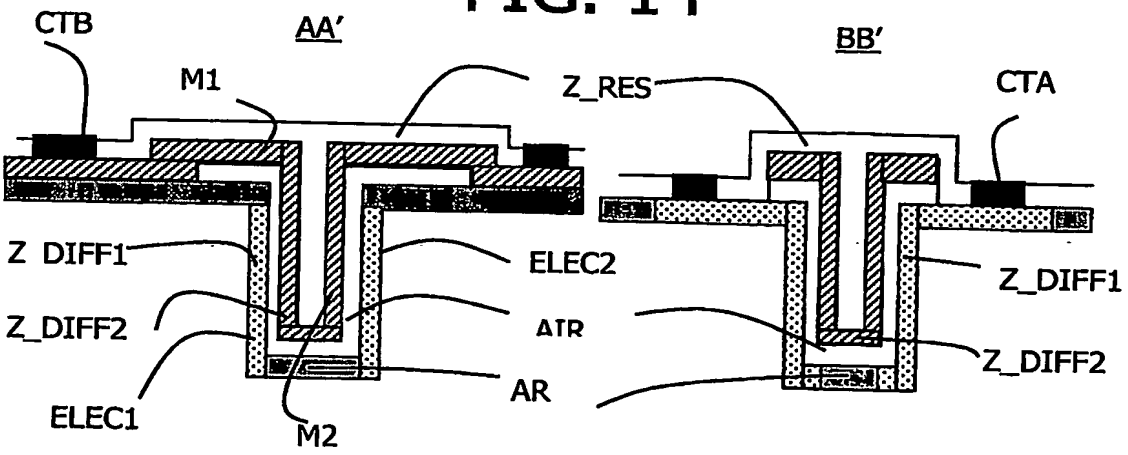
CTB
AA'
BB'
M1
Z_RES
CTA
Z_DIFF1
ELEC2
Z_DIFF1
Z_DIFF2
ATR
Z_DIFF2
AR
ELEC1
M2

FIG. 15